N-channel 950 V, 1 Ω typ., 6 A MDmesh™ K5 Power MOSFET in a H²PAK-2 package

Datasheet - production data

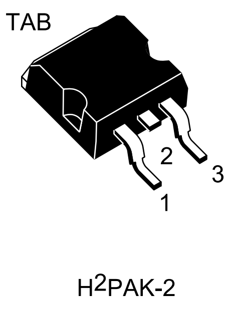
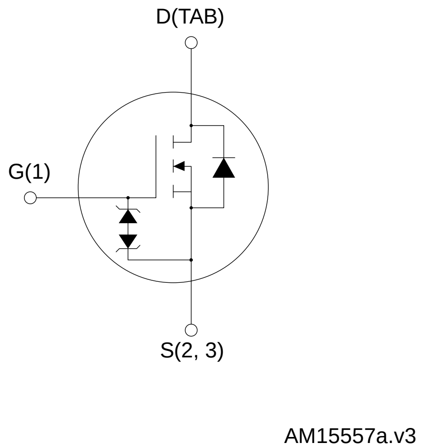


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STH6N95K5-2	950 V	1.25 Ω	6 A	110 W

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STH6N95K5-2	6N95K5	H²PAK-2	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current at T_C = 25 °C	6	A
I_D	Drain current at T_C = 100 °C	3.8	A
I_{DM}(1)	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
I_{AR}(2)	Max current during repetitive or single pulse avalanche	3	A
E_{AS}(3)	Single pulse avalanche energy	90	mJ
dv/dt(4)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt(5)	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature	- 55 to 150	°C
T_{stg}	Storage temperature		

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulse width limited by T_{jmax}.

(3)Starting T_j = 25 °C, I_D = I_{AS}, V_{DD} = 50 V.

(4)I_{SD} ≤ 6 A, di/dt ≤ 100 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$.

(5)V_{DS} ≤ 760 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.14	°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb max	30	

Notes:

(1)When mounted on 1 inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	950			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 950 V			1	µA
		V_{GS} = 0 V, V_{DS} = 950 V, T_c = 125 °C			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{CS} = 10 V, I_D = 3 A		1	1.25	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	450	-	pF
C_{oss}	Output capacitance		-	30	-	
C_{oss}	Output capacitance		-	1.6	-	
$C_{o(tr)}$ (1)	Equivalent capacitance, time-related	V_{GS} = 0 V, V_{DS} = 0 to 760 V	-	45	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance, energy-related		-	19	-	
R_G	Intrinsic gate resistance	f = 1 MHz, I_D =0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 6 A, V_{GS} = 10 V (see *Figure 16: "Gate charge test circuit"*)	-	13	-	nC
Q_{gs}	Gate-source charge		-	3	-	
Q_{gd}	Gate-drain charge		-	7	-	

Notes:

(1)Time-related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

(2)Energy-related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 475 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	12	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off-delay time		-	33	-	ns
t_f	Fall time		-	21	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM}[(1)]	Source-drain current (pulsed)		-		24	A
V_{SD}[(2)]	Forward on voltage	I_{SD} = 6 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs V_{DD} = 60 V	-	372		ns
Q_{rr}	Reverse recovery charge		-	4		µC
I_{RRM}	Reverse recovery current		-	22		A
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C	-	522		ns
Q_{rr}	Reverse recovery charge		-	5		µC
I_{RRM}	Reverse recovery current		-	20		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

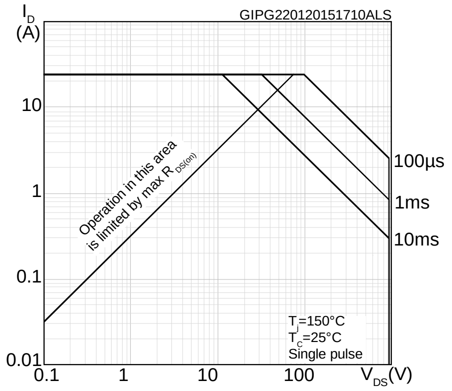


Figure 3: Thermal impedance

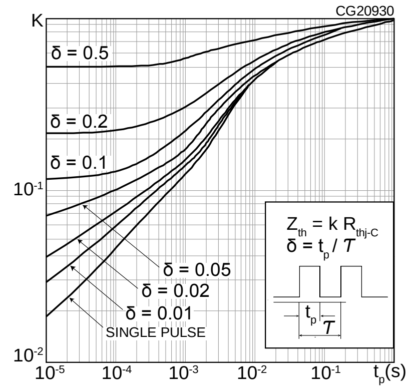


Figure 4: Output characteristics

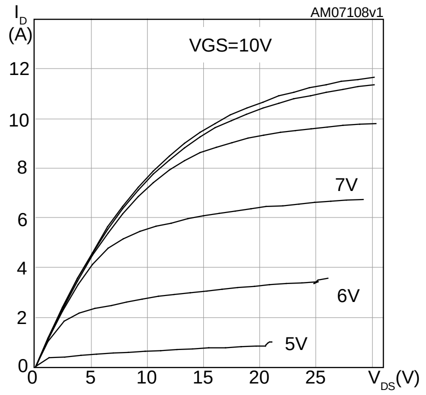


Figure 5: Transfer characteristics

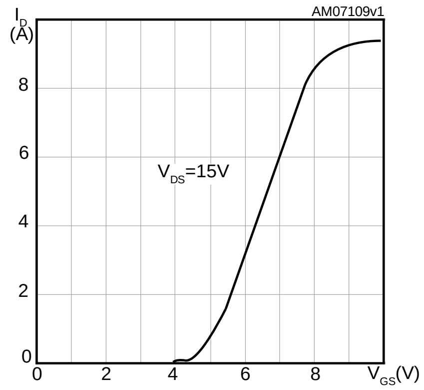


Figure 6: Gate charge vs gate-source voltage

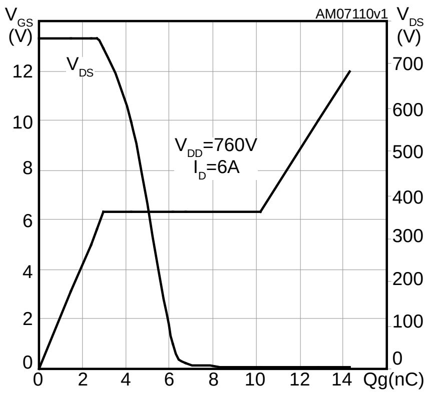


Figure 7: Static drain-source on-resistance

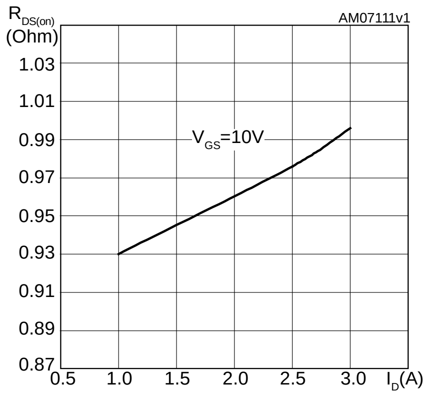


Figure 8: Capacitance variations

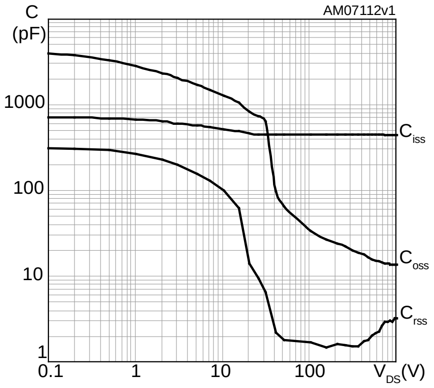


Figure 9: Output capacitance stored energy

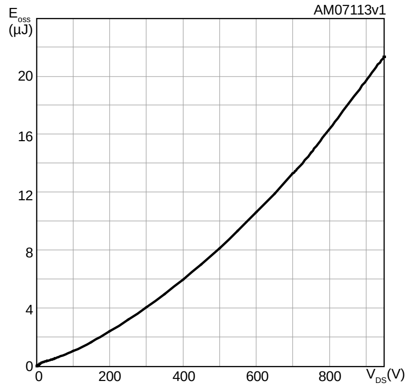


Figure 10: Normalized gate threshold voltage vs temperature

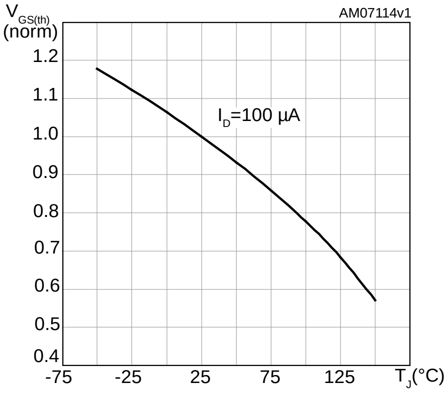


Figure 11: Normalized on-resistance vs temperature

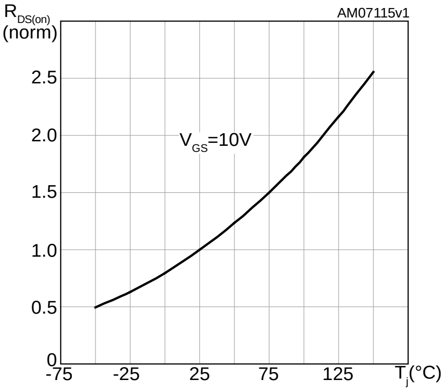


Figure 12: Source-drain diode forward characteristics

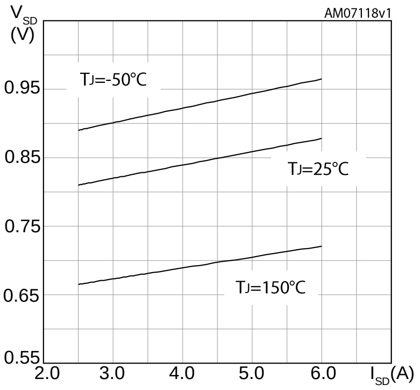


Figure 13: Normalized V(BR)DSS vs temperature

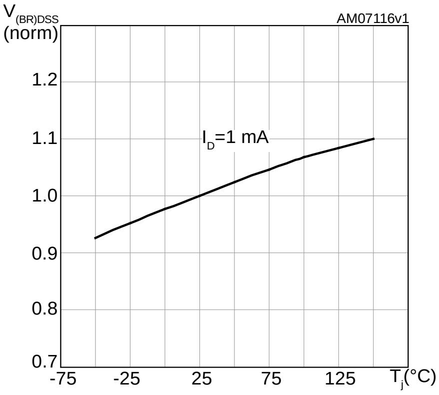
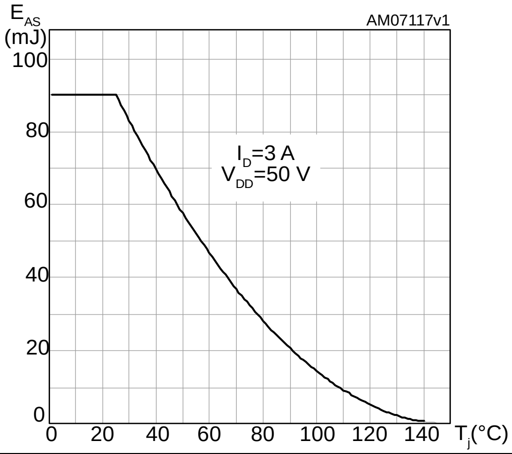


Figure 14: Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 15: Switching times test circuit for resistive load

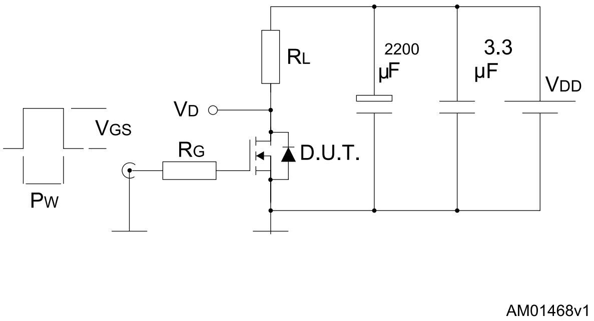


Figure 16: Gate charge test circuit

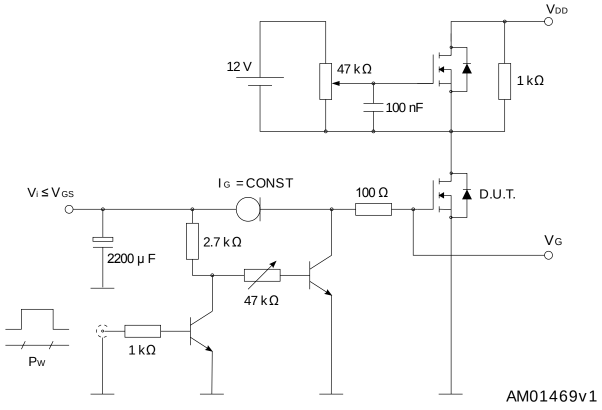


Figure 17: Test circuit for inductive load switching and diode recovery times

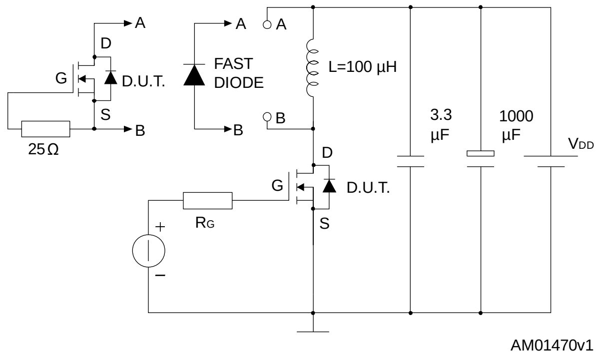


Figure 18: Unclamped inductive load test circuit

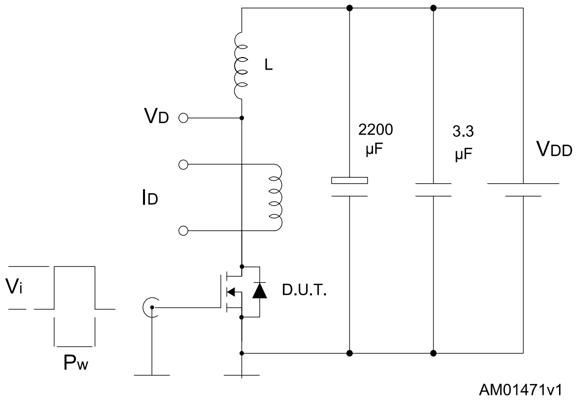


Figure 19: Unclamped inductive waveform

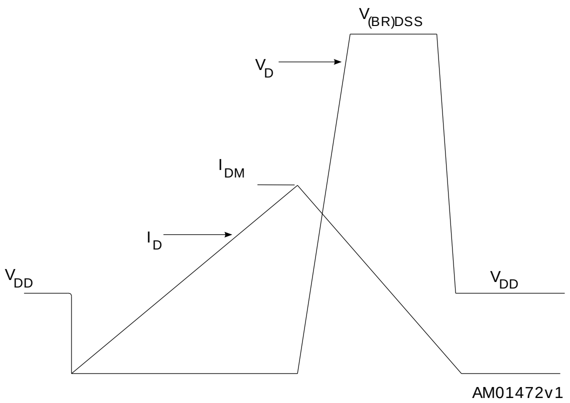
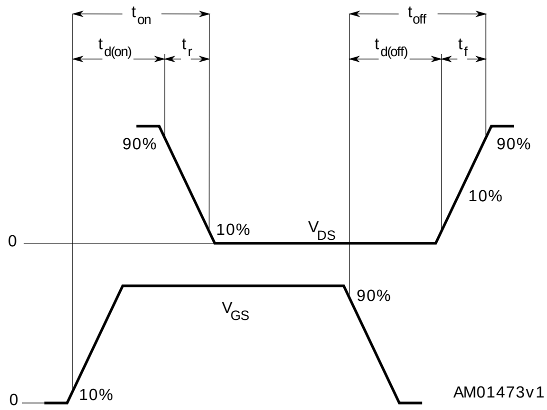


Figure 20: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 Package mechanical data

Figure 21: H²PAK-2 outline

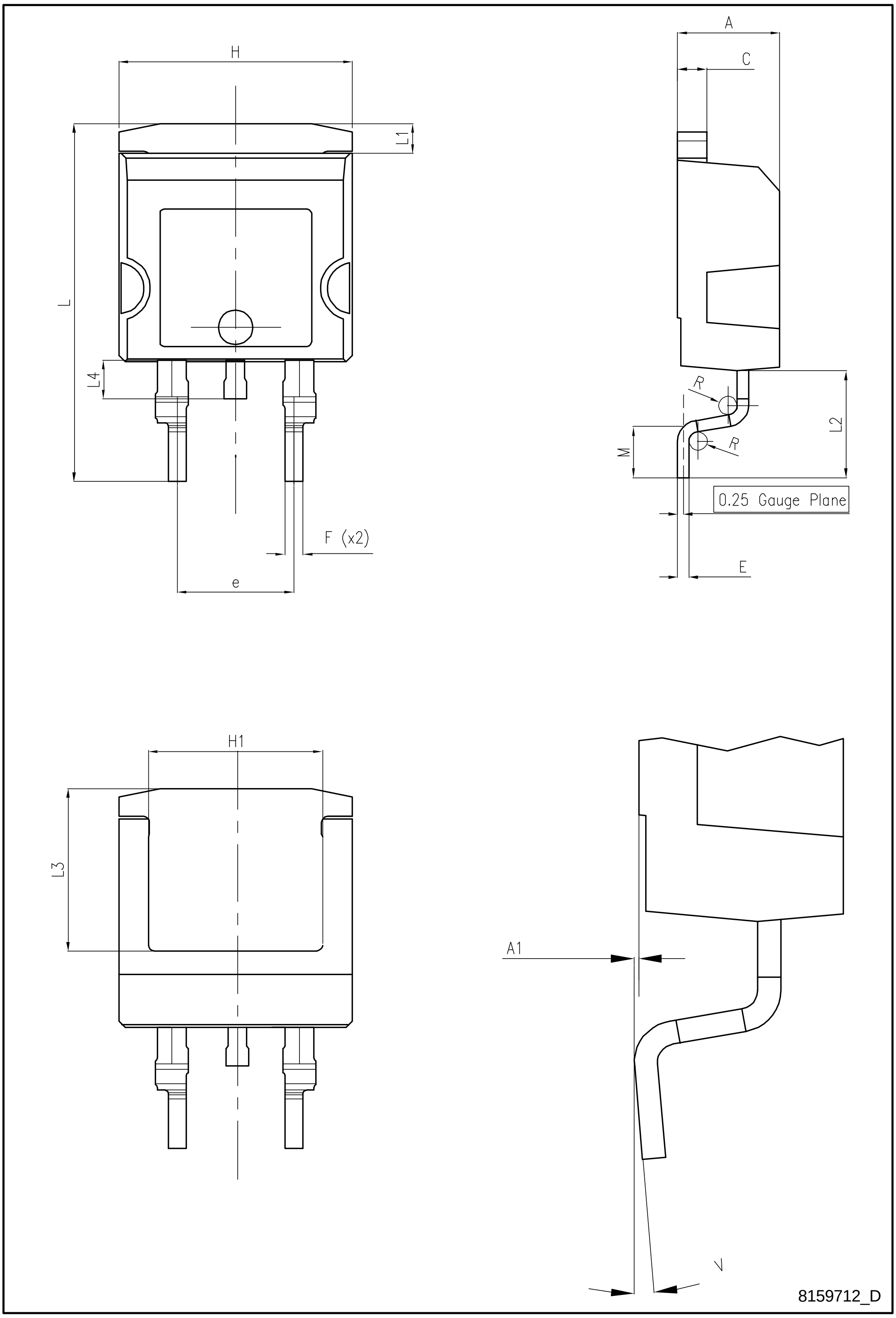
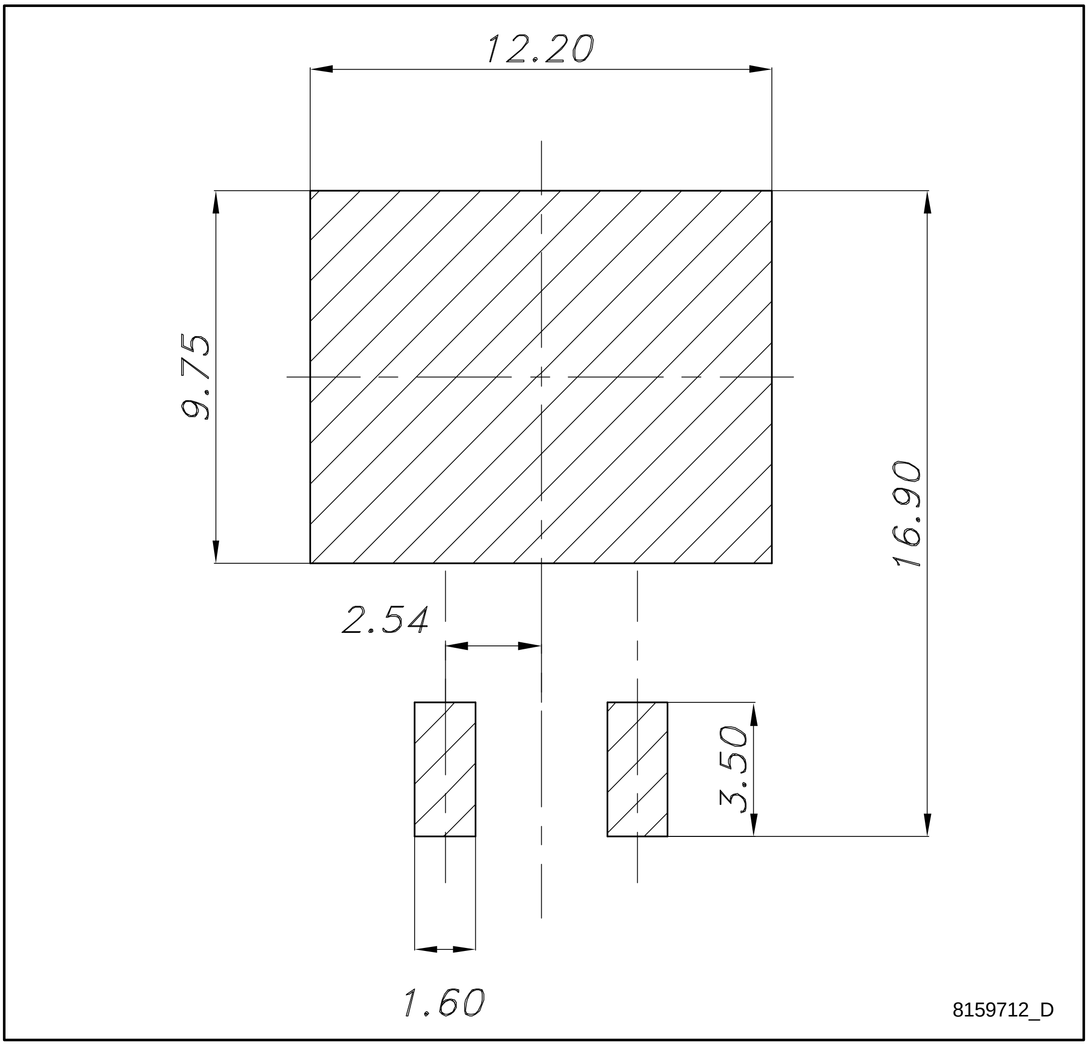


Table 9: H²PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 22: H²PAK-2 recommended footprint



5 Packing information

Figure 23: Tape outline

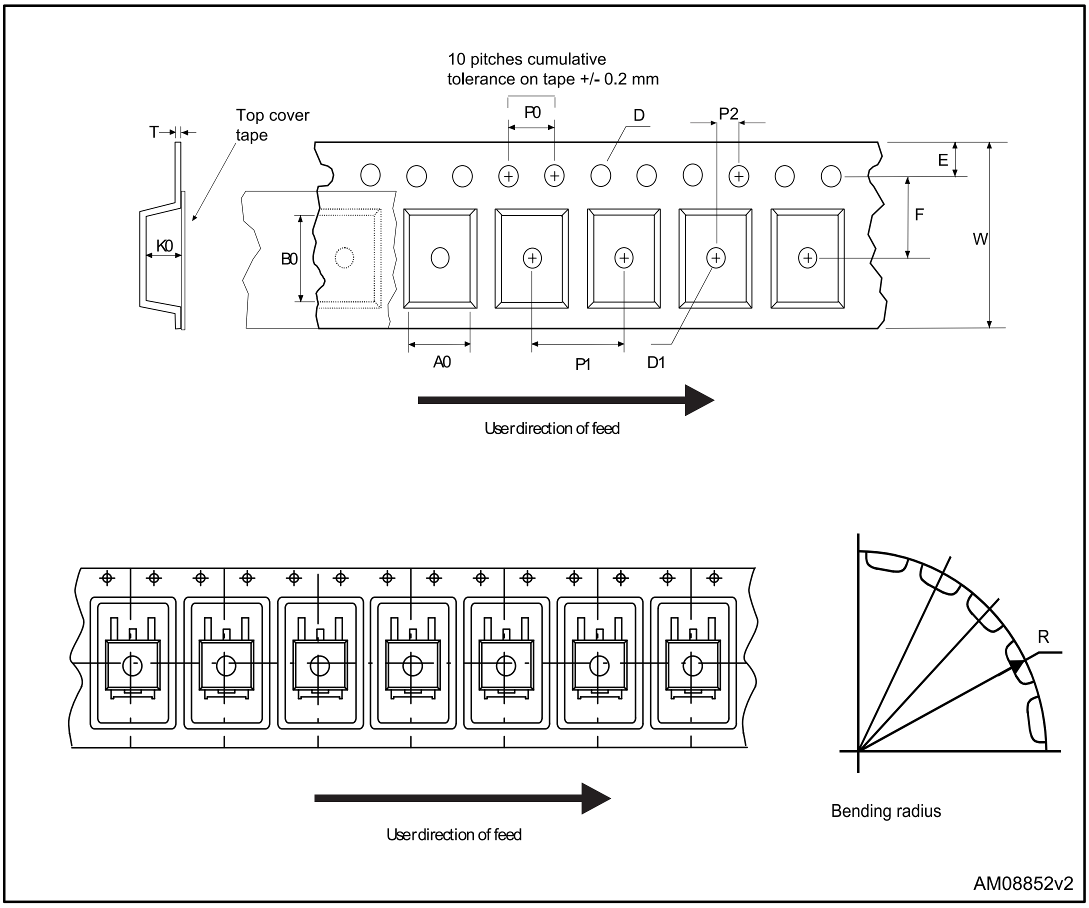


Figure 24: Reel outline

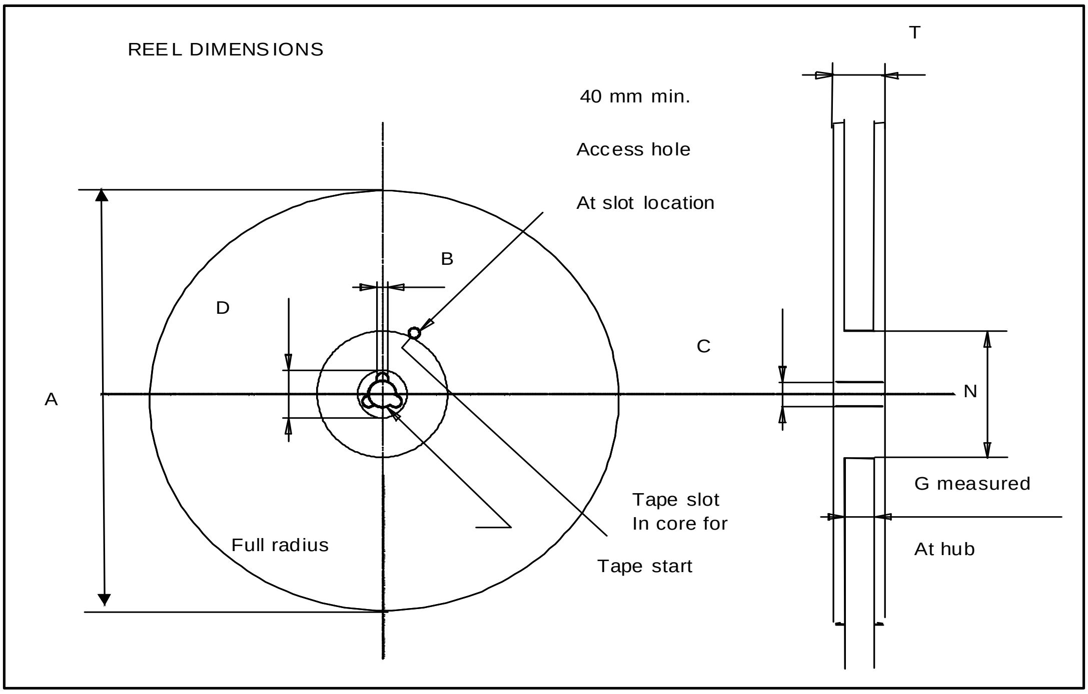


Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 11: Document revision history

Date	Revision	Changes
23-Jan-2015	1	First release.
04-Feb-2015	2	Updated *Section 2: "Electrical characteristics"*
12-Mar-2015	3	Document status changed from preliminary to producion data.